IN THE SPECIFICATION:

Please amend paragraph **[0009]** as follows:

[0009] Referring to FIG. 2B, the crystallized silicon layer (i.e., a polysilicon layer) is patterned to from an island-shaped active layer 16. The polysilicon active layer 16 is divided into a [[fist]] first portion 16a and second portions 16b. The first portion 16a is located in the middle of the polysilicon active layer 16, and the second portions 16b are located on both right and left sides of the first portion 16a. The first portion 16a is often referred to as an active portion, and the second portions 16b are often referred to as ohmic contact portions. A gate insulation layer 18 is formed on the buffer layer 12 to cover the polysilicon active layer 16. The gate insulation layer 18 is made of silicon oxide (SiO_2) using a Plasma Enhanced Chemical Vapor Deposition (PECVD) method.

Please amend paragraph **[0038]** as follows:

[0038] Referring to FIG. 6B, the crystallized silicon layer (i.e., a polysilicon layer) is patterned to form an island-shaped active layer 106. The polysilicon active layer 106 is divided into a [[fist]] first portion 106a and second portions 106b. The first portion 106a is located in the middle of the polysilicon active layer 106, and the second portions 106b are located on both right and left sides of the first portion 106a. The first portion 106a is often referred to as an active

portion, and the second portions 106b are often referred to as ohmic contact portions. A gate insulation layer 108 is formed on the buffer layer 102 to cover the polysilicon active layer 106. The gate insulation layer 108 is made of silicon oxide (SiO_2) using a Plasma Enhanced Chemical Vapor Deposition (PECVD) method in a vacuum chamber for example.